UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,095	12/02/2003	Jong-Hyun Choi	8021-172 (SS-18277-US)	3428

22150 7590 11/02/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,095	CHOI ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Aug 8, 2005 (Amdt) & Sep 16, 2005 (IDS)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10* is/are allowed.

6)☒ Claim(s) *1-9, and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09162005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/IDS

The amendment submitted on Aug 8, 2005, and the IDS submitted on Sep 16, 2005, were reviewed and considered with the following results:

The amended changes to the disclosure overcame the objections described in the previous Office Action. Therefore, those objections have been withdrawn.

Amended claims 1 and 2 overcame the previous rejections of claims 1-10 under 35 U.S.C. 112. Although those rejections have now been withdrawn, amended claim 1 created a new problem with respect to claim 2. This rejection is described later under the appropriate section.

Amended claim 1 also overcame the rejection of claim 1 under 35 U.S.C. 102(b) with respect to Park, and the rejections of claims 1-9 under 35 U.S.C. 103(a) with respect to Jang and Lim et al. These rejections have been withdrawn because the references do not show a distributing unit having an enabling switch with its control terminal connected to the external power supply voltage as now recited within claim 1, and/or because the Lim reference has the same assignee, and therefore has been removed from consideration with respect to the present application. However, claims 1-9 have now been rejected under the Jang reference, in view of a reference by Yamasaki. These rejections are described later under the appropriate section.

Amended claim 10 is now allowed.

Newly added claims 28-31 are rejected under the appropriate section described later.

The prior art reference cited on the IDS does not clearly show/disclose the clamping control unit of claims 1 and 10, nor the comparison means of newly added claim 28.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Since claim 1 now has an enabling switch in the distributing unit, how do the first-fourth transistors of claim 2 relate to it? Using the applicant's own Fig. 1 as a reference, the enabling switch of claim 1 corresponds to transistor TR4, wherein the first-fourth transistors correspond to transistors TR1-TR4. Therefore, isn't claim 2's fourth transistor the enabling switch of claim 1? Claims 3-7 carry over the rejection from claim 2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Newly added claims 28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Park, a reference cited in the previous Office Action. Fig. 3 shows mode means MN21-MN23 for controlling a voltage level of at least one of a first (Vreftrim), second (Vref1), and third (COM) voltage in response to at least one operating mode signal CODE1-CODE3; comparison

means 52 for comparing the first and second voltages; and adjusting means R21-R25,MN24 for effectively controlling the voltage level of third voltage COM in response to at least one of the mode means and comparison means, anticipating claim 28. The mode means comprises control unit MN21-MN23; comparison means comprises differential amplifier unit 52; and adjusting means comprises distributing unit R21-R25,MN24. Therefore, claim 30 is also anticipated.

Newly added claims 28 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Shokouhi et al. Fig. 1 shows one type of a voltage generating circuit comprising mode means M01-M03,MS1-MS11,R1-R30 for controlling a voltage level of at least one of a first (e.g. applied to the + input of 102), second (ground), and third (e.g. the output of charge pump 105 that is not shown); comparison means 102 (and M01-M03,MS1-MS11,R1-R30) for comparing the first and second voltages; and adjusting means 105 for controlling the voltage level of the third voltage in response to at least one of the mode means and the comparison means. The signal(s) that control whether any one of the elements within mode means M01-M03,MS1-MS11,R1-R30 is open or closed is deemed at least one type of an operating mode signal. Therefore, claim 28 is anticipated. Mode means comprises voltage level detecting unit M01-M03,MS1-MS11,R1-R30; comparison means comprises the voltage level detecting unit, along with differential amplifier 102; and adjusting means comprises boosting unit 105. This anticipates claim 31.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, and newly added claims 28-29, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang (a reference cited in the previous Office Action) in view of Yamasaki, a reference found during a recent update search. Fig. 1 of Jang shows reference voltage generating circuit 100 comprising distributing unit R1-R5,M1-M20 for generating reference voltage VREF via an output terminal (not labeled but understood to be the node between R1 and R2), wherein VREF is lower than external power supply voltage VDD, and selectively varied according to an operating mode (e.g. which combination of fuses F1-F9 are blown/used); clamping control unit 103, connected between the output terminal and ground voltage VSS, for clamping a voltage level of reference voltage VREF in response to control voltage A that is lower than reference voltage VREF; and control unit F1-F11 for selectively increasing or decreasing a level of reference voltage VREF. At least one of elements M13-M20, within the distributing unit, can be considered an enabling switch with a control terminal connected to external power supply voltage VDD. Although the reference shows a plurality of means (i.e. F1-F11) for selectively varying reference voltage VREF, the reference does not clearly show or disclose the response to

first/second operating mode signals. Yamasaki shows and discloses another type of reference voltage generating circuit that generates a reference voltage that can be selectively varied with respect to a distributing unit and mode signals. For example, Fig. 7 shows distributing unit 4a,R5-R10, and control unit P1-P4, wherein Fig. 8 shows the same distributing unit 4a,R5-R10, but Fig. 7's the control unit comprising fuses P1-P4 has been replaced by control transistors T1-T4, along with their corresponding control signals. Therefore, it would have been obvious to one of ordinary skill in the art to modify Jang's reference voltage generating circuit by replacing each fuse F1-F11 with its own respective control transistor/control (e.g. operating mode) signal to either utilize, or bypass, its corresponding resistive element. Thus, the control unit can increase or decrease reference voltage VREF in response to (at least) first/second operating mode signals, rendering claim 1 obvious. The use of only fuses, as shown in Jang reference, provides a means for selectively adjusting reference voltage VREF on a more permanent basis, wherein once a fuse is blown (or cut), it remains an open and its corresponding resistive element cannot be bypassed. However, additional fuses can be blown/cut at a later time. By using a corresponding transistor/control signal instead of a fuse, the level of reference voltage VREF can be selectively controlled in a temporary, more controllable manner. For example, if it was determined VREF should be at a higher or lower value, due to element degradation over time and temperature, the appropriate combination of transistors could be turned on and off to obtain the desired reference voltage VREF. The distributing unit of Jang comprises first resistor R1 connected between external power supply voltage VDD and the output terminal; second resistor R2-R5 connected between the output terminal and a first node from which control voltage A is output; at least first through third transistors (e.g. any three of transistors M1-M12), and a fourth transistor (e.g. any

one of transistors M13-M20), are connected in series between the first node and ground voltage VSS. The control terminals of the first through third transistors (e.g. any three of M7-M12) are connected to the output terminal, and the external power supply voltage is applied to the control terminal of the fourth transistor (e.g. any one of M13- M20). Therefore, claim 2 is rendered obvious. Since all of transistors M1-M20 are NMOS transistors, claim 3 is also rendered obvious. One of ordinary skill in the art would understand the controlling of the width-to-length ratio of each of transistors M1-M20 would control the level of reference voltage VREF, rendering obvious claim 4. [For example, once the circuit is fabricated, the physical W/L ratio of each transistor is set, and maximum/minimum levels of reference voltage VREF can be generated (e.g. when all of the resistive elements are used (i.e. not bypassed) within the series current path, a maximum level of reference voltage VREF will be generated; and when all the resistive elements with their corresponding bypass means (e.g. fuse or transistor) are bypassed, the minimum level of reference voltage VREF will be generated. Any other combination of how many resistive elements are bypassed will allow the reference voltage generating circuit to generate a selected level of reference voltage VREF that is between the maximum and minimum levels.] Deeming any one of the transistors, and its control signal, as the first control transistor, and its first operating mode signal, respectively; and deeming any one of the other transistors, and its control signal, as the second control transistor, and its second operating mode signal, respectively, claim 5 is rendered obvious. The signals will allow its respective control transistor to be either turned on or off, thus allowing the corresponding resistive element to be either bypassed, or used, providing a means for selectively increasing or decreasing the level of reference voltage VREF. Using R7/T2/Ø1 and R6/T1/Ø2 of Yamasaki's Fig. 8 as an example, it

would have been obvious to one of ordinary skill in the art to use an NMOS transistor as the first control transistor coupled in parallel (e.g. source to source, and drain to drain) to the first transistor (e.g. a first resistive device), with the first operating mode signal applied to the NMOS transistor's gate, rendering claim 6 obvious. For similar reasons, it would have been obvious to one of ordinary skill in the art to use an NMOS transistor as the second control transistor coupled in parallel (e.g. source to source, and drain to drain) to the third transistor (e.g. a third resistive device), with the second operating mode signal applied to the NMOS transistor's gate, rendering claim 7 obvious. Since clamping control unit 103 comprises PMOS transistor M31 with its first/second ends coupled between the output terminal and ground voltage VSS, and its gate receiving control voltage A, claim 8 is also rendered obvious. MRS signals are known to be one type of command signals that can be used to determined the operational status of a circuit. Therefore, deeming Yamasaki's control signals as mode register set type signals, claim 9 is also rendered obvious since they will be used to set (or command) which particular elements within Jang's distributing unit are to be used or bypassed. Interpreting the references of Jang/Yamasaki in a different manner, mode means (e.g. corresponding to fuses F1-F11 being replaced by control transistors/control signals of Yamasaki) controls a voltage level of at least one of a first (e.g. VDD), a second (e.g. at node A), and a third (e.g. VREF) voltage in response to at least one operating mode signal; comparison means effectively compares the first voltage with the second voltage; and adjusting means 103 controls third voltage VREF in response to at least one of the mode means and comparison means, rendering claim 28 obvious. Since the mode means comprises a control unit (e.g. control transistors/control signals), the comparison means

comprises distributing unit R1-R5,M1-M20, and adjusting means comprises clamping control unit 103, claim 29 is also rendered obvious.

Claims 11-27 have been cancelled.

Allowable Subject Matter

Claim 10 is allowed. None of the prior art references reviewed and considered show a voltage generating circuit as recited within independent claim 10, wherein the circuit requires the first/second operating mode signals being at their appropriate first/second levels for the low, high, and intermediate operating frequency ranges as recited within claim 10.

Prior Art

Although not used in any formal rejections described above, the other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least sections of the claimed invention. For example, Fig. 17 of Kuriyama shows a voltage generating circuit comprising control unit 90 and mode signals Mode1-Mode4; differential amplifier unit OP90,OP91,QN90, QN91,QP90, QP91; and distributing unit Rload,Rref. Therefore, this reference should be carefully reviewed and considered with respect to the broadest reasonable interpretation of the claimed limitations.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

28 October 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800